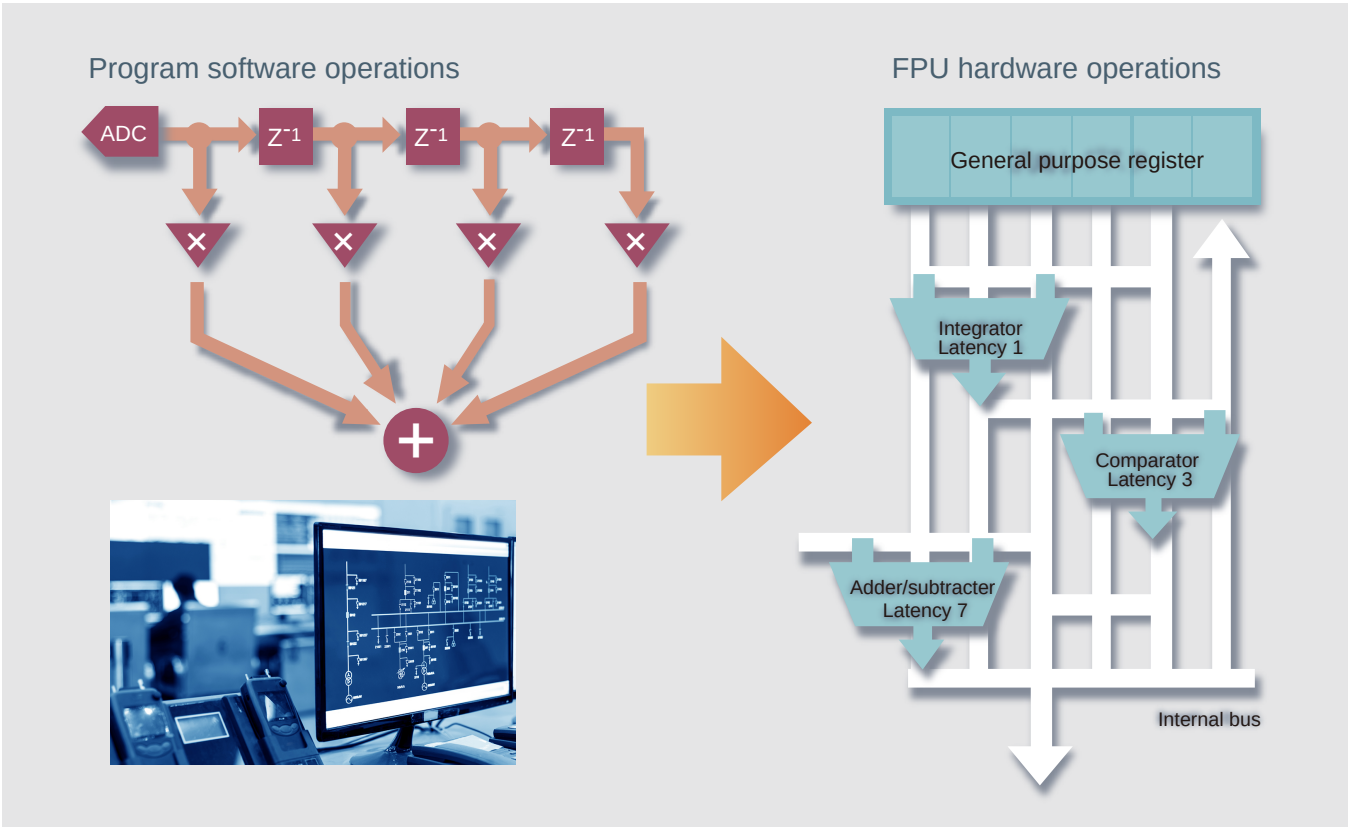
Hardware design | FPGA design | Research equipment/facilities

IEEE 754 compliant 32-bit floating point operations unit

A floating point FIR operations circuit has been implemented using FPGA to speed up the algorithms in the existing C source. This unit is being used as an IP in the FPGA designed by the client.



Development

- A floating point FIR operations circuit is implemented using FPGA, and the algorithms from the existing C source are speeded up
- This unit is used as an IP in the FPGA designed by the client

Features

- Inbuilt IEEE 754 32-bit compliant floating point operations unit
- Specially customized high-performance pipeline structure to ensure that existing operating formulae in C can run at high speed
- Optimized structure which runs using a small capacity, low speed CLK, and yet completes processing within the prescribed time